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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,843	07/21/2003	Veronika Polei	P2002,0618	6526

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,843	POLEI ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *072103* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claims 3, 6, and 7 are objected to because of the following informalities:

In claim 3, line 1, replace "claims" with --claim--;

In claim 6, line 1, replace "claims" with --claim--;

In claim 7, line 1, replace "claims" with --claim--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. (U.S. Patent 6,326,268).

In re claim 1, **Park** discloses a method for fabricating a buried bit line for a semiconductor memory, which comprises: producing strip-like doped regions parallel to and at distances from one another semiconductor body, the regions being adapted to act as bit lines and as source/drain regions of a respective memory transistor (col. 3, lines 3-59 and **FIGS. 2-7**); applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric and including a lower boundary layer **(FIG. 3: 36)**, a storage layer **(FIG. 3: 38)**, and an upper boundary layer **(FIG. 7: 48)** (col. 3, line 36 to col. 4, line 48); forming an oxide region **(FIG. 2: 22)** in each case on a side of the doped regions remote from the semiconductor body **(FIG. 3: 24)** (col. 3, lines 3-

16), the oxide region being thicker than the lower boundary layer (element **22** is thicker than element **36**) (col. 4, lines 42-63); before the upper boundary layer is applied, applying a sacrificial layer (**32** and **40**) made from polysilicon and a material selectively etchable with respect to a material of the storage layer to the storage layer (col. 3, lines 47-59); producing openings **(FIG. 3)** the sacrificial layer **40**, the storage layer **38**, and the lower boundary layer **36**, extending the semiconductor body **24**, by using a mask (col. 3, lines 48-59); introducing doped polysilicon into the openings; removing the sacrificial layer **(FIG. 4)**; and producing the upper boundary layer **(FIG. 7: 48)** on the storage layer 46 and oxidizing at least a proportion of the polysilicon to form the oxide region **(FIG. 7: 22)** (col. 4, lines 11-63).

In re claim 2, **Park** discloses wherein the sacrificial layer is produced as a deposited oxide (col. 4, lines 11-21 and **FIG. 4**).

In re claim 3, **Park** discloses wherein the method according claim 1 which further comprises selecting the storage layer (**38** and **46**) from a group of materials consisting of silicon nitride, tantalum oxide, hafnium oxide, hafnium silicate, titanium oxide, zirconium oxide, aluminum oxide, and intrinsically conductive silicon (col. 3, lines 48-59) and (col. 4, line 42-48).

2. Claims 4-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. (U.S. Patent 6,326,268).

In re claim 4, **Park** discloses a method for fabricating a buried bit line for a semiconductor memory, which comprises: producing strip-like doped regions parallel to

and at distances from one another semiconductor body, the strip-like doped regions being adapted to act as bit lines and as source/drain regions of a respective memory transistor (col. 3, lines 3-59 and **FIGS. 2-7**); applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric and including a lower boundary layer **(FIG. 3: 36)**, a storage layer **(FIG. 3: 38)**, and an upper boundary layer **(FIG. 7: 48)** (col. 3, line 36 to col. 4, line 48); and forming an oxide region **(FIG. 2: 22)** thicker than the lower boundary layer in each case on a side of the doped region remote from the semiconductor body **(FIG. 3: 24)** (col. 3, lines 3-16) (element **22** is thicker than element **36**) (col. 4, lines 42-63); before producing the upper boundary layer, applying a sacrificial layer (**32** and **40**) with a topside to the storage layer (col. 3, lines 47-59); producing openings **(FIG. 3)** with lateral walls in the sacrificial layer **40**, the storage layer **38**, and the lower boundary layer **36** by using a mask (col. 3, lines 48-59); introducing dopant into the implantation regions of the semiconductor body through the openings (col. 3, line 60 to col. 4, line 21); etching back the lateral walls of the openings and the topside of the sacrificial layer at an etching rate sufficient to form smooth sides on the sacrificial layer, the storage layer, and the lower boundary layer (col. 4, lines 34-41); removing residues of the sacrificial layer selectively with respect to the storage layer **(FIG. 4)**; and producing the upper boundary layer **(FIG. 7: 48)** on the storage layer **46** and forming an oxide region **(FIG. 7: 22)** on a free surface of the semiconductor body, in each case between the sides (col. 4, lines 11-63).

In re claim 5, **Park** discloses wherein the method according to claim 4, which further comprises heating until the dopant introduce into the implantation regions has

diffused to a portion of the semiconductor body covered by the storage layer (col. 4, lines 11-41).

In re claim 6, **Park** discloses wherein the sacrificial layer is produced as a deposited oxide (col. 4, lines 11-21 and **FIG. 4**).

In re claim 7, **Park** discloses wherein the method according claim 4 which further comprises selecting the storage layer (**38** and **46**) from a group of materials consisting of silicon nitride, tantalum oxide, hafnium oxide, hafnium silicate, titanium oxide, zirconium oxide, aluminum oxide, and intrinsically conductive silicon (col. 3, lines 48-59) and (col. 4, line 42-48).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
July 8, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER